Boundary-Scan Software Aids PCB Evaluation

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IEEE 1149.1 tools generate synthesizable boundary-scan-circuit descriptions, and when a foundry converts them to silicon, the resulting boundary-scan circuits help find manufacturing flaws on PCBs.

Last month, I described some design-for-test tools that help you build testable ICs.[1] This month, I'll look at complementary software tools that insert boundary-scan circuitry into ICs. This circuitry reduces the test chores from in-circuit board testers, reducing the pin count on bed-of-nails fixtures.

Boundary-scan circuitry includes scan cells inserted in series with each I/O pin of an IC. A single scan cell can serve a basic unidirectional pin. Three-state and bidirectional pins require more cells (**Fig. 1**). During normal operation, the cells are transparent to the normal flow of data between an IC's data pins and its internal logic. In test mode, scan-cell latches provide the data, either to exercise internal chip logic or to drive an output pin. In the latter case, a test system can probe the other end of the PCB trace to which that output pin connects in an effort to verify trace continuity.

The scan-cell latches receive their test data by means of the four-pin test-access port (TAP) defined in the IEEE 1149.1 standard.[2] The pins include a test-mode-select (TMS) pin, a test-clock signal (TCK), and test-data input (TDI) and test-data-output (TDO) pins. When asserted, TMS enables the scan circuitry on each I/O pin of a boundary-scan-compliant DUT (for example, by putting the switches in Fig. 1 in the lower position). With TMS active, TCK clocks data serially into TDI, from which scan-cell latches acquire their data. TDO provides a path to the TDI of additional ICs on a PCB.

During test, the TAP signals are exercised by TAP controller hardware, available from a variety of firms.[3] The TAP also can serve to carry programming information into PLDs, allowing simultaneous testing and programming—called in-system programming (ISP)—of PCB-mounted PLDs.[4,5]

Indeed, PLDs are a prime target for boundary-scan techniques, and PLD makers including Altera (San Jose, CA) and Xilinx (San Jose, CA) offer tools that help implement boundary-scan circuitry within their chips. Xilinx, for example, has released a Java application programming interface (API) for boundary scan as part of its Silicon Xpresso initiative announced last fall.[6] The free Xilinx software package includes a reference implementation of the API, plus source code and Xilinx XC9500 CPLD algorithms that use this API. It also includes a translator that accepts boundary-scan descriptions in serial vector format (SVF) to create Java API-based applications.

In an effort to establish a standard file format for ISP, Altera freely licenses its Jam programming and test language. Jam includes two software components: a Jam composer that writes the Jam file required to program a specific design into a specific device, and a

(text continues on p. 69)

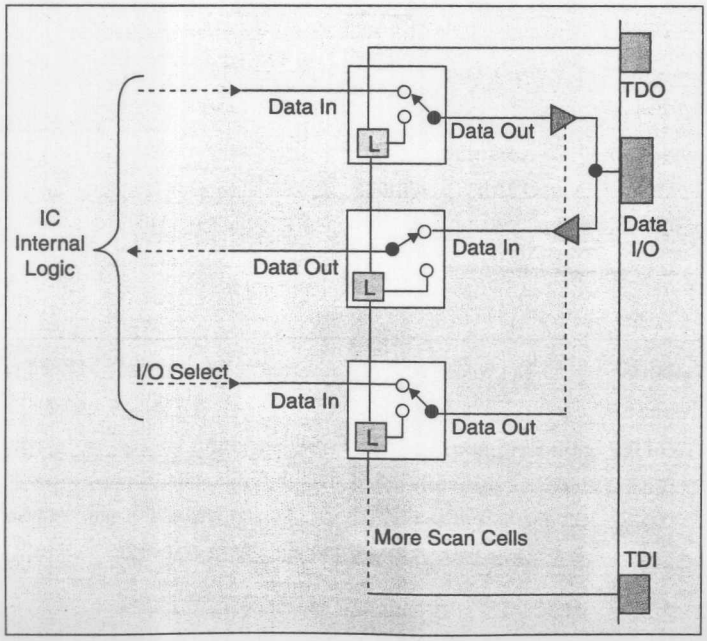

FIGURE 1 Bidirectional data pins can require three scan cells. In normal operation (with switches as shown), data flows transparently between IC internal logic and the bidirectional pin buffer; the IC's internal I/O Select function determines whether the pin handles data input or output. In test mode, the state of the latch (L) in the bottom cell determines data direction. If input mode is selected, the contents of the middle latch exercise internal logic; if output is selected, the contents of the top latch drive the external Data I/O pin and the PCB trace to which it connects.

T&MW Product Survey: Representative Boundary-Scan Software Tools

Company	Tool	Modeling Language or EDA Environment	Output Format or Instrument Compatibility	Comment
Acugen Nashua, NH *603-881-8821* *www.acugen.com* **TIX 221**	PROGBSDL	BSDL plus PLD design files	BSDL	Converts a BSDL file for an unprogrammed PLD into a BSDL file for a programmed PLD, declaring certain pins as unused or input-only.
		BSDL	Test vectors	Reads a BSDL file and generates a high-fault-coverage test program for an in-circuit or component tester.
ASSET-InterTech Richardson, TX *972-437-2800* *www.asset-intertech.com* **TIX 222**	ScanConnect	EDIF plus proprietary netlist formats from Mentor, Viewlogic, and Cadence.	Test vectors	Automatic interconnect pattern generation verification of boundary-scan -to-boundary-scan interconnects provides fault diagnosis to the net level.
	ScanDetect	BSDL, HSDL, SVF	Fault-diagnosis reports	Detects and reports errors; indicates open and bad bidirectional cells.
	ScanObjects	C, C++	C, C++, SVF	Programmer's tool for creating custom test applications.
Corelis Cerritos, CA *562-926-6727* *www.corelis.com* **TIX 223**	ScanPlusTPG	Netlists, BSDL	Test patterns, VCL files	Generates interconnect test patterns that provide 100% fault coverage of scannable nets.
	ScanPlus Runner	Vector Control Language files	Test programs, test reports	Test executive to help develop a test sequence or plan from various independent tests.
	ScanPlus Debugger		Graphical interface	Supports debug during prototype-design-verification and testing.
Goepel Electronic Jena, Germany *+49-3641-6896-63* *www.goepel.com* **TIX 224**	System Cascon	BSDL, SVF, various CAE design-file formats	Test patterns, test programs, documentation	Suite of tools for CAE-file import, design-verification, ATPG, test-program generation, and emulation.
JTAG Technologies Eindhoven, the Netherlands *+31 40 295 08 70* *www.jtag.com* **TIX 225**	JTAGLINK	CAE design files	ATPG input data schematic system to JTAG	Interfaces specific EDA Technologies' test-pattern-generation tools.
	JTAGTEST	EDIF or JTAGLINK data	Test vectors, test programs and reports, pin-level repair information	Performs boundary-scan test preparation, test execution, and test-results analysis.
	ActiveTest	EDIF	Test vectors	Reads an EDIF and a list of IEEE 1149.1-compliant parts; presents a summary of PCB nets indicating direction as input, output, or I/O.
LogicVision San Jose, CA *408-453-0146* *www.lvision.com* **TIX 226**	jtag-XLi	Verilog, VHDL, SVF	RTL Verilog, VHDL	Inserts at-speed boundary-scan cells as well as at-speed interconnect test controllers into synthesizable designs.
Mentor Graphics Wilsonville, OR *800-547-3000* *www.mentor.com* **TIX 227**	BSDArchitect	VHDL, Verilog	VHDL, Verilog, BSDL	Inserts boundary-scan circuitry into a behavioral-level VHDL or Verilog description of an IC, ASIC, or MCM design.
Syntest Sunnyvale, CA *408-720-9956* *www.syntest.com* **TIX 228**	TurboBSD	Verilog, VHDL	Verilog, VHDL	Generates test-bench and synthesizable RTL code for boundary-scan insertion.

the target device.

Corelis has added support for Jam to its ScanPlus boundary-scan development, manufacturing, and field-service-test systems. The platform-independent Corelis ScanPlus software (which includes a Jam Player) can program onboard devices such as Altera's MAX 7000 and MAX 9000 chips using Corelis JTAG controllers for the ISA bus, the PCI bus, the PC Card bus, or LAN.

Of course, boundary scan is not limited to PLDs; you can employ IEEE 1149.1 techniques on any digital part you design. A variety of software tools (see the **product survey chart**, p. 66) can help you implement boundary-scan circuits in your designs no matter what format your design data is in—including EDIF, Verilog, VHDL, or proprietary netlist formats.

Traditionally, boundary-scan testing has been the domain of test and production engineers wishing to check the integrity of assembled PCBs by using the built-in test possibilities offered by JTAG-compliant ICs. This has required them to follow a formal test-development program involving ATPG tools that required cryptic netlist and component data formats.

JTAG Technologies is trying to make boundary-scan test easier for designers and test engineers to use by enabling access to a PCB's boundary-scan features via an interactive Windows GUI. Its ActiveTest software hides the details of TAP states, BSDL data files, and serial shift sequences.

By reading an EDIF 200 netlist of your design along with a list of JTAG-compliant parts, ActiveTest presents a summary of PCB nets, highlighting which nets can be accessed through boundary-scan and indicating whether a pin is input only, output only, or bidirectional. Test patterns can be assigned to groups of nets using binary, hex, octal, or decimal bases. Vectors are then assigned a direction and can be executed in a single step or continuous loop modes. Logic-analyzer-style state or timing diagrams then can be used to display vector updates and vector captures. *T&MW*

SOCs." *T&MW,* September, 1999, p. 32.

2. 1149.1 *IEEE Standard Test Access Port and Boundary-Scan Architecture.* IEEE, Piscataway, NJ, *www.ieee.org.*

3. "Boundary-Scan Tools Keep Pace with Device Innovations," *T&MW,* November 1998, p. 41.

4. "Careful PCB Layout Enhances Onboard Programming," *T&MW,* January 1999, p. 49.

6. "Initiative Moves Boundary-Scan Tool to Web," *T&MW,* October 1998, p. 6.

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